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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/733,605
Filing Date: December 11, 2003
Appellant(s): JOHNSON, GARY M.

Jaison C. John
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/16/2007 appealing from the Office action mailed 1/08/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,483,359	Lee	11-2002
6,445,231	Baker et al	09-2002
5,101,117	Johnson et al	04-1992

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 9-10, 35-38 and 43-44 are rejected under 35 USC 103 (a) as being unpatentable over Lee (US 6,483,359) in view of Johnson et al (US 5,101,117).

Regarding claims 1 and 35, Lee discloses in Figures 3-7 a delay lock loop circuit (DLL) being used in a memory device to provide an output signal (DLL_CLK) based upon a phase difference between a reference signal (EXT_CLK) and a feedback signal from a delay monitor (310). Said delay lock loop comprises a delay circuit (340) which includes capacitors (C1-C3) coupled to inverters (341, 344) through switches (345-347) to provide delays when the capacitors (C1-C3) are activated by the switches (345-347).

Regarding claims 2-3 and 36, wherein said device is a memory device (SRAM), see lines 10-23, column 1.

Regarding claims 4 and 37, wherein said delay lock loop further comprises:

-a coarse delay unit (340) to provide a coarse delay upon at least one of said reference signal (EXT_CLK) and a data output signal;

- a fine delay unit (360) to provide a fine delay upon at least one of said reference signal (EXT_CLK) and said data output signal;

-the phase detector (320) to detect said phase difference; and

- a feedback delay unit (310) operatively coupled to said coarse delay unit (340) to generate said

feedback signal.

Regarding claim 9, wherein said output signal (DLL_CLK)comprises said coarse delay and said fine delay.

Regarding claim10, wherein said reference signal is the clock signal (EXT_CLK).

Regarding claim 38, wherein said fine delay unit (360) comprises at least one delay block (364-366, Figure 4) for providing a delay upon at least one of said reference signal and said data output signal.

However, Lee does not disclose that the capacitor (C1-C3) are the transistors (transistive capacitors) for providing "a transitive capacitive delay" as called for in claims 1, 25 and 35.

Nevertheless, Johnson et al suggests in Figure 1 a delay lock loop circuit and a delay circuit (22) in Figure 4 comprising transistive capacitors (72a-72l) coupled to inverters (70a-70l) through switches (71a-71l) for providing transistive capacitive delays when the transistive capacitors (72a-72l) are activated by the switches (71a-71l). Wherein the transistors (72a-72l) are connected to function as capacitors and are used in the delay circuit for easily being implemented on an integrated circuit since the transistors are the semiconductor devices. The conventional capacitors have very large size so that they cannot be implemented on the integrated circuit.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the transitive capacitors as suggested by Johnson et al in the circuit of Lee for the purpose of allowing the capacitors to be implemented on an integrated circuit in order to reduce the size of the delay lock loop circuit.

Claims 1-4, 9-10, 25-28, 33-38 and 43-44 are rejected under 35 USC 103 (a) as being

unpatentable over Baker et al (US 6,445,231) in view of Lee (US 6,483,359)) and further in view of Johnson et al (US 5,101,117).

Baker et al discloses in Figures 1, 2A, 3A and 12-15, a system comprising:
- a first device (110) having a memory device (102, Figure 1) for storing data and a delay lock loop circuit (311) to provide an output signal based upon a phase difference between a reference signal (CLKin) and a feedback signal (CLKout) as shown in Figures 2A and 3A, and
- a second device (112 in Figure 2, or 1502 in Figure 15) operatively coupled to said first device (102) to access said data (203) from said first device (102) based upon an operation performed by said delay lock loop (111), see Figure 2A.

However, Baker does not disclose that the DLL circuit (111) comprising a delay circuit for activating transistive capacitive delay as called for in claims 1, 25 and 35.

Nevertheless, Lee in view of Johnson et al suggests the modified delay lock loop with the modified delay circuit for activating a transistive capacitive delay as stated above for providing a finer adjustability that would reduce jitters, see lines 5-9, column 1 of the Lee reference.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the modified DLL circuit of Lee in view of Johnson in the circuit of Baker et al for the purpose of providing a finer adjustability that would reduce jitters.

Allowable Subject Matter

Claims 5-8, 29-32 and 39-42 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims. These claims are allowed because the

prior art of record fails to suggest "the delay circuit comprising the inverters and the transistor sets" in combination as claimed.

(10) Response to Argument

1). The Appellant argues at page 5 of the Appeal Brief that Lee is directed to a passive capacitor that may be connected to the inverted clock signal, and does not disclose a transistive capacitive delay for use in a delay circuit of a delay lock loop. Johnson does not make up for the lack of disclosure of Lee because Johnson is directed to passive capacitors. Therefore, neither of these prior art references suggest using a transistive capacitive delay for a delay circuit in a delay lock loop. The arguments are not persuasive because of the following reasons:

i). There is nothing recited in the rejected claims anything about "active capacitors" or "passive capacitors". For example, independent claims 1, 25 and 35 of the present invention only recite that the delay lock loop comprises "a delay circuit for activating a transistive capacitive delay" and Figure 5 of the present invention only shows that the delay circuit comprising unmarked transistive capacitors (transistors being connected to function as capacitors) coupled to inverters (510, 58) through unmarked switches to provide delays for the delay circuit when they are activated by the unmarked switches. Thus, the claimed limitation "transistive capacitive delay" does not recite anything about "active capacitors" or "passive capacitors". This claimed limitation is interpreted as a delay provided by a transistive capacitor (a transistor being connected to function as a capacitor) when the transistive capacitor is activated that is clearly shown on Figure 4 of Johnson et al in which the delay circuit (22)

comprises transistive capacitors (72a-72l) being activated by the switches (71a-71l) to provide delays.

ii). Since the delay circuit of Johnson has the structure similar to the structure of the claimed delay circuit of the present invention, both delay circuits would perform the same function.

iii). Johnson employs the transistors (72a-72l) to perform the function of capacitors so that the transistors (72a-72l) are considered as active capacitors because the transistors are active devices.

2). The Appellant argues that Baker clearly does not disclose the delay circuit for activating a transistive capacitor delay and the cited prior art references, alone or in combination, do not make obvious all of the elements of claims of the present invention. The arguments are not persuasive because the modified delay lock loop of Baker in view of Lee and Johnson would provide "a delay circuit for activating a transistive capacitive delay" as stated above.

3). The Appellant argues at page 6-7 that, under the Examiner's theory, even a light bulb that is switched by a gate switch would become an active transistive device and passive capacitive may or may not be activated by a different set of switches does not make them transistive capacitances. Johnson, does not make up for this deficit for various reasons because Johnson simply discloses passive capacitors (72a-72l). The argument are not persuasive because of the flowing reasons:

i). The light bulb is not a transistor or a transistive device so that it cannot become a transistive device after being activated by a gate switch.

ii). The capacitors (72a-72l) of Johnson are active capacitors because they are transistors.

4). The Appellant argues at the second paragraph of page 8 of the Appeal Brief that combining Johnson and Lee is improper hindsight reasoning to combine practically any prior art reference to tailor arguments for obviousness. The arguments are not persuasive because it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

5). The Appellant argues at the first paragraph of page 9 of the Appeal Brief that Johnson does not disclose a feedback signal for using the phase detector. Therefore, Johnson is entirely different and non-analogous to Lee and those skilled in the art would not be motivated to combine them to make obvious all of the elements of claims of the present invention. The arguments are not persuasive because of the following reasons:

i). Figure 1 of Johnson et al clearly shows that the signal (19) is the feedback signal which is provided for a phase detector (30) from a delay line (22)/

ii). Since Lee discloses in Figures 3-4 a delay lock loop circuit comprising a delay circuit for providing an output clock signal and Johnson also disclose in Figures 1 and 4 a delay lock loop circuit comprising a delay circuit (Figure 4) for providing an output clock signal, both Lee reference and Johnson reference are analogous art.

iii). The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the

knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Lee discloses in Figures 3-7 a delay circuit (340) comprising switches (345-347) and capacitors (C1-C3) coupled to inverters (341, 344) but does not disclose that the capacitors (C1-C2) are the transistors for providing "transistive capacitive delay". While Johnson et al suggests in Figures 1-3 and 4 a delay circuit comprising transistive capacitors (72a-72l) for easily being implemented on an integrated circuit. Thus, a person having skill in the art would have been motivated to employ the transitive capacitors as suggested by Johnson et al in the circuit of Lee for the purpose of allowing the capacitors to be implemented on an integrated circuit in order to reduce the size of the delay lock loop circuit.

6). The Appellant argue at page 8 of the Appeal Brief that the Examiner incorrectly identifies the capacitors 72a-721 in Figure 4 of Johnson as a transistive capacitor because the capacitors shown in Figure 4 (72a-721) are actually simple passive capacitors whose connection is influenced by the transistors (71 a-71l). Johnson clearly discloses that the delay line in Figure 4 consists of a series of drivers and control transistors 71a-711 and 12 capacitors 72a-721. See, column 4, lines 39-44. Therefore, neither Lee nor Johnson discloses or makes obvious a transistive capacitor. The arguments are not persuasive because the transistive capacitors (72a-72l) of Johnson are active capacitors as stated above. Thus, the modified delay circuit of Lee in view of Johnson et al would provide a "transistive capacitive delay".

7). The appellant argues at page 12 of the Appeal Brief that there is no motivation to combined Baker with Lee and/or Johnson. The arguments are not persuasive because the examiner recognizes that obviousness can only be established by combining or modifying the

teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Baker et al discloses in Figures 1, 2A, 3A and 12-15 a system board comprising a memory device (102, Figure 1) for storing data and a delay lock loop circuit (311) to provide an output signal based upon a phase difference between a reference signal (CLKin) and a feedback signal (CLKout) as shown in Figures 2A and 3A but does not disclose that that the DLL circuit (111) comprises a delay circuit for activating a transistive capacitive delay. While Lee in view of Johnson et al suggests the modified delay lock loop with the modified delay circuit for activating a transistive capacitive delay as stated above for providing a finer adjustability that would reduce jitters. Thus, a person having skill in the art would have been motivated to employ the modified DLL circuit of Lee in view of Johnson in the circuit of Baker et al for the purpose of providing a finer adjustability that would reduce jitters.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is 571-272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards. can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent (Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

Drew Richards

David Blum

DINH T. LE
PRIMARY EXAMINER

10 October 2007